

What is claimed is:

1. A semiconductor integrated circuit device comprising:  
writable and readable memory cells;  
an address selector circuit for subjecting said memory cells to selection;  
a write circuit for conveying write signals to memory cells selected by said address selector circuit;  
a read circuit for conveying read signals from memory cells selected by said address selector circuit; and  
a timing generator circuit which receives a clock signal and generates operational timing signals to be conveyed to said address selector circuit, write circuit and read circuit,  
wherein any circuit in which the operational timing is not too tight is configured of a higher threshold voltage MOSFET than the MOSFETs of other circuits.
2. The semiconductor integrated circuit device according to Claim 1,  
wherein said memory cells are configured of said higher threshold voltage MOSFETs, and  
wherein said circuit in which the operational timing is not too tight is comprised of a circuit which gives operational timing signals to an output circuit contained in said read circuit.
3. The semiconductor integrated circuit device according to Claim 2,

wherein said circuit in which the operational timing is not too tight comprises a write amplifier which is included in said write circuit and generates write signals, a column switch exclusively for writing which is included in said address selector circuit, and a circuit for conveying a selection signal to the column switch.

4. The semiconductor integrated circuit device according to Claim 3,

wherein said memory cells are static memory cells provided at the intersections of complementary bit lines and word lines, and

wherein said complementary bit lines and read complementary read signal lines include as said circuit in which the operational timing is not too tight a precharger/equalizer circuit configured of said higher threshold voltage MOSFET.

5. The semiconductor integrated circuit device according to Claim 1,

wherein said circuit in which the operational timing is not too tight comprises a write amplifier which is included in said write circuit and generates write signals, a column switch exclusively for writing which is included in said address selector circuit, and a circuit for conveying a selection signal to the column switch.

6. The semiconductor integrated circuit device according to Claim 5,

wherein said memory cells are static memory cells provided at the intersections of complementary bit lines and word lines, and

wherein said complementary bit lines and read complementary read signal lines include as said circuit in which the operational timing is not too tight a precharger/equalizer circuit configured of said higher threshold voltage MOSFET.

7. A semiconductor integrated circuit device comprising:  
writable and readable memory cells;  
an address selector circuit for subjecting said memory cells to selection;

a write circuit for conveying write signals to memory cells selected by said address selector circuit;

a read circuit for conveying read signals from memory cells selected by said address selector circuit; and

a timing generator circuit which receives a clock signal and generates operational timing signals to be conveyed to said address selector circuit, write circuit and read circuit,

wherein each of the drive circuits for conveying operational timing signals to large load capacities is configured of a higher threshold voltage MOSFET of a greater channel width than the MOSFETs of other circuits, and causes drive currents matching the load capacities to flow.

8. The semiconductor integrated circuit device according to Claim 7,

wherein the drive circuits for conveying operational timing signals to large load capacities are a word driver and a driver supplying timing signals having a greater number of fan-outs.

9. The semiconductor integrated circuit device according to Claim 8,

wherein said circuit in which the operational timing is not too tight is comprised of said higher threshold voltage MOSFET.

10. The semiconductor integrated circuit device according to Claim 9,

wherein said memory cells are comprised of said higher threshold voltage MOSFETs, and

wherein said circuit in which the operational timing is not too tight is comprised of a circuit for giving operational timing signals to an output circuit included in said read circuit.

11. The semiconductor integrated circuit device according to Claim 10,

wherein said circuit in which the operational timing is not too tight comprises a write amplifier which is included in said write circuit and generates write signals, a column switch exclusively for writing which is included in said address selector circuit, and a circuit for conveying a selection signal to the column switch.

12. The semiconductor integrated circuit device according to Claim 11,

wherein said memory cells are static memory cells provided

at the intersections of complementary bit lines and word lines,  
and

wherein said complementary bit lines and read complementary read signal lines include as said circuit in which the operational timing is not too tight a precharger/equalizer circuit configured of said higher threshold voltage MOSFET.

13. A semiconductor integrated circuit device comprising:  
writable and readable memory cells;  
an address selector circuit for subjecting said memory cells to selection;

a write circuit for conveying write signals to memory cells selected by said address selector circuit;

a read circuit for conveying read signals from memory cells selected by said address selector circuit; and

a timing generator circuit which receives a clock signal and generates operational timing signals to be conveyed to said address selector circuit, write circuit and read circuit,

wherein said read circuit has a data output latch circuit and a data output buffer,

wherein said timing generator circuit has a first circuit for giving a latch timing signal to said data output latch circuit, and a second circuit for giving a data output timing signal to said data output buffer, and

wherein the output transistors of said first and second circuits are made greater in size and their threshold voltages

are higher than those of the transistors constituting other circuits.

14. The semiconductor integrated circuit device according to Claim 13,

wherein a plurality of sets of said data output latch circuits and said data output buffers are provided.

15. The semiconductor integrated circuit device according to Claim 14,

wherein said memory cells is comprised of the higher threshold voltage MOSFETs.

16. The semiconductor integrated circuit device according to Claim 15,

wherein said address selector circuit has a word line driver circuit for driving word lines, and

wherein other circuits than the final stage circuit of said word line driver circuit are configured of lower threshold voltage transistors.

17. The semiconductor integrated circuit device according to Claim 15,

wherein said memory cells are static memory cells provided at the intersections of complementary bit lines and word lines, and

wherein said complementary bit lines and read complementary read signal lines include as said circuit in which the operational timing is not too tight a precharger/equalizer circuit configured

of said higher threshold voltage MOSFET.